Ultra Wide Band Low Noise Amplifier for Communication Receivers in 0.18 µm CMOS technology

Maryam Vafadar

***Abstract*— This paper presents an inductorless low-noise amplifier (LNA) design for an ultra-wideband (UWB) receiver frontend. A current-reuse gain-enhanced noise canceling architecture is proposed, and the properties and limitations of the gainenhancement stage are discussed. Capacitive peaking is employed to improve the gain flatness and 3-dB bandwidth, at the cost of absolute gain value. The LNA circuit is fabricated in a 0.18-µm triple-well CMOS technology. Measurement result good matching in the implementations and a small-signal gain of 11 dB and a 3-dB bandwidth of 2–9.6 GHz are obtained. The LNA consumes 19 mW from a low supply voltage of 1.5 V. It is shown that the LNA designed without on-chip inductors achieves comparable performances with inductor-based designs. The silicon area is reduced significantly in the inductorless design, the LNA core occupies only 0.05 mm2, which is among the smallest reported designs.**

***Index Terms*— Low Noise Amplifier (LNA), RF integrated circuit (RFIC), Ultra-WideBand (UWB), CMOS technology, noise cancellation, gain enhancement, Matching.**

I. INTRODUCTION

Today everywhere around us radio signals and systems coexist and operate side by side such as GSM, 3G, WLAN, Bluetooth, FM-radio and many more.the standard of ultra-wideband (UWB) was set up by the Federal Communications Commission (FCC) in 2002. The FCC authorized the unlicensed 7.5-GHz band (3.1–10.6 GHz) for UWB applications. Motivated by implementing the transceivers with low cost and a high integration level, CMOS technology becomes the most attractive candidate. Owing to the rapid progress of CMOS technology, many studies of CMOS RF integrated circuits (RFICs) for UWB applications were published in succession with good results [1]–[6].

Low-Noise Amplifier (LNA) is the first stage in a receiver after the antenna. Its purpose is to amplify the desired signal as much as possible without adding noise or consuming too much power. In an UWB receiver, the LNA with a wideband operation capability is critical to the overall receiver performance. The bandwidth of the LNA is ultimately limited by the parasitic capacitances of the devices. The demand for power efficient, accurate and small transmitters and receivers grows and is a big research field worldwide. Inductors, occupy a large chip area. The solution has been to use inductors off and on chip. Another problem is to obtain a good impedance match between the antenna and the LNA input.

Maryam Vafadar, Department of Electronic, Sama technical and vocational training college, Islamic Azad University, Islamshahr Branch, Islamshahr, Iran

This paper demonstrates the feasibility of inductorless LNA design capable of UWB applications. A gain-enhanced architecture based on noise canceling principle is studied Fabricatedin a 0. 18-µm triple-well CMOS process, the LNA achieves a small signal gain of 11-dB and a -3-dB bandwidth of 2-9.6-GHz with Sll<-15-dB in-band impedance matching. The LNA consumes 19-mW from a low supply voltage of 1.5 V. The performaces are comparable and sometimes better than inductor-based designs. The inductorless architecture saves area significantly, the LNA occupies only 0.05 mm2, which is among the smallest UWB LNA designs.

This paper presents a UWB LNA with comprehensive considerations on NF and wideband gain performance. noise sensing and canceling architecture is exploited, which employs a current-reuse stage for gain compensation. Inductorless design is also explored. Bandwidth enhancement is achieved by capacitive peaking. Section II presents a literature review of previous works on LNA designs. Section III presents a modified wideband noise canceling architecture capable of higher gain performance, approaches to bandwidth enhancement are discussed and an inductorless approach using capacitive peaking is presented. We implement three types of circuit architectures and Section IV shows the experimental results of the demonstrated LNA circuits. This paper is finally concluded in Section V.

II. LITERATURE REVIEW

Traditionally, types of wideband amplifiers were implemented with balanced or distributed architectures that were originally used in microwave circuit design [1]–[3]. However, the large area occupation and high power dissipation of the traveling-wave amplifier make it infeasible for low-power single-chip integration. Recently, a distributed amplifier has been reported in [4], which achieves comparable performance with lumped design in terms of power and area consumption. With the development of advanced semiconductor technology, lumped implementation of the LNA in CMOS and SiGe BiCMOS has been pushed up to tens of gigahertz [5], [6]. There are also a few UWB LNAs that have been reported in the literature. Various circuit techniques have been proposed to enhance the bandwidth.

A classical approach to widening bandwidth is negative feedback, which is normally realized in the form of resistive shunt feedback [7-8]. The feedback can also be implemented using an active circuit [9] or a transformer [10]. Meanwhile, standalone negative feedback can hardly achieve sufficient bandwidth; the inductor peaking technique is often adopted in these feedback-based designs. Further, the analysis presented in [11] shows that resistive feedback amplifiers cannot provide required performance with low power consumption.

In [12-13], UWB LNAs with multisection impedance matching are reported, which expand the use of an inductor-degenerated amplifier with emphasis on wideband impedance matching. This approach is efficient in terms of bandwidth and has been proven in both CMOS and SiGe BiCMOS technologies. However, the extra passive devices used for matching purpose increase design complexity and area occupation. Recently, a combined feedback architecture for UWB LNA design has been reported [7], [14], [15]. Adopted from microwave circuits [16], [17], the resistive feedback is applied both globally and locally.

This architecture achieves sufficient bandwidth and gain even without inductors. However, potential instability problem occurs due to multiple feedback loops. High transconductance device is also required for bandwidth–gain tradeoff. Thus, this configuration has not been realized in standard CMOS technology. Compared with narrowband LNA designs, a severe tradeoff between NF and source impedance matching exists in a wideband LNA. Most of the reported UWB LNA designs are focused on bandwidth enhancement. As a result, a few of them achieve comparable noise performance with narrowband LNAs. A CMOS UWB LNA employing the noise-canceling technique is reported in [18], where thermal noise of the input matching device can be sensed and canceled by the feed-forward configuration [19]. This avoids potential instability due to global negative feedback. However, the gain performance of such a configuration is often less superior.

III. GAIN-ENHANCED WIDEBAND NOISE CANCELING ARCHITECTURE

The wideband LNA design exploiting thermal noise canceling was originally presented by Bruccoleri *et al.* [20], [21]. the noise combining stage can also be designed using a wideband transformer [22], where the amplification is achieved at the cost of silicon area instead of power. However, is still limited by the noise canceling condition, and the use of transformer limits the bandwidth of the LNA.

In this paper, we implement three three types of circuit architectures as follows:

A. Circuit Architecture Type one

A gain-enhanced noise canceling architecture is presented here. The purpose of gain enhancement is not only on improving the gain of noise canceling architectures, but also on creating more freedom in tradeoffs involving gain. As the inductorless approach will be explored in this paper, parasitic capacitances cannot be driven with an inductor-peaking method. To achieve ultra-wide bandwidth, extensive tradeoff between bandwidth and gain may be required. Thus, a higher gain configuration offers more flexibilities for such tradeoff.

Fig. 1 shows the modified architecture of a wideband noise canceling LNA. A current-reused amplification stage, and *C*2 is adopted between the noise sensing and combining stages. *C*2 is a large decoupling capacitor that creates a ground node at RF. This stage provides two feed-forward paths concurrently. Meanwhile, the current reuse permits higher efficiency of power and available voltage headroom [30].

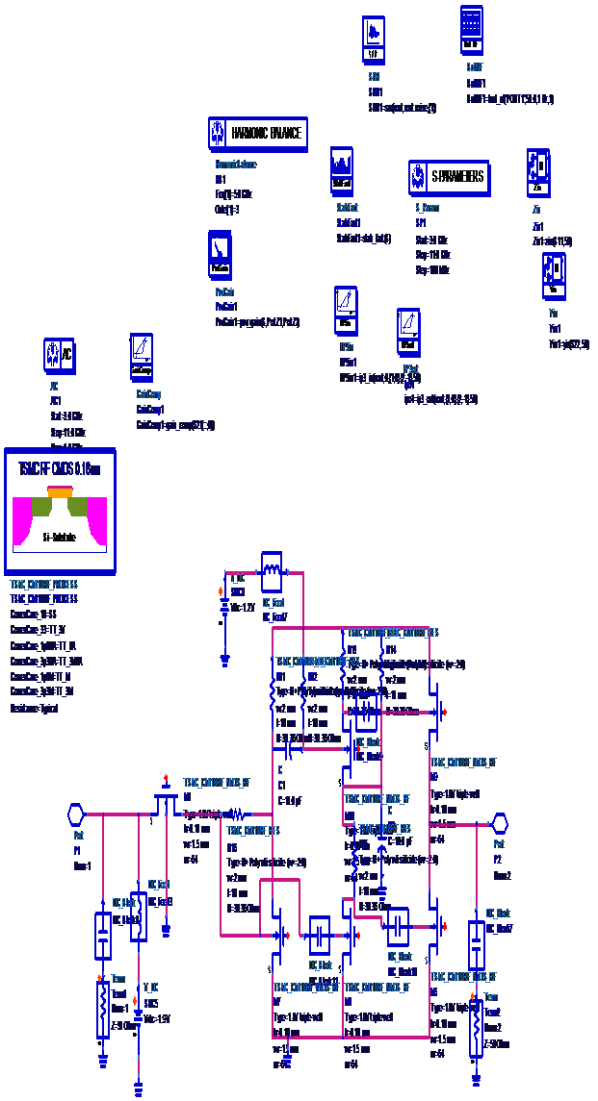


Fig. 1. Circuit Architecture Type One

Note that the input parasitic capacitance degrades both input matching and noise sensing [18], [22]. As the target frequency of the design is up to 10 GHz, it is important to keep the input parasitics as small as possible.

B. Circuit Architecture Type two

An on-chip inductor is widely used to improve the bandwidth performance of the broadband LNA. For the proposed circuit in Fig. 1, inductors L1=0.6nH and L2=1.5nH can also be used for bandwidth extension. A possible example is shown in Fig. 2, where and are employed in the input stage. Furthermore, the input matching and noise performance are improved significantly. This is because the input capacitance is the dominate limitation for both impedance matching and noise sensing, the inductors in the input stage decrease such an effect at high frequencies.

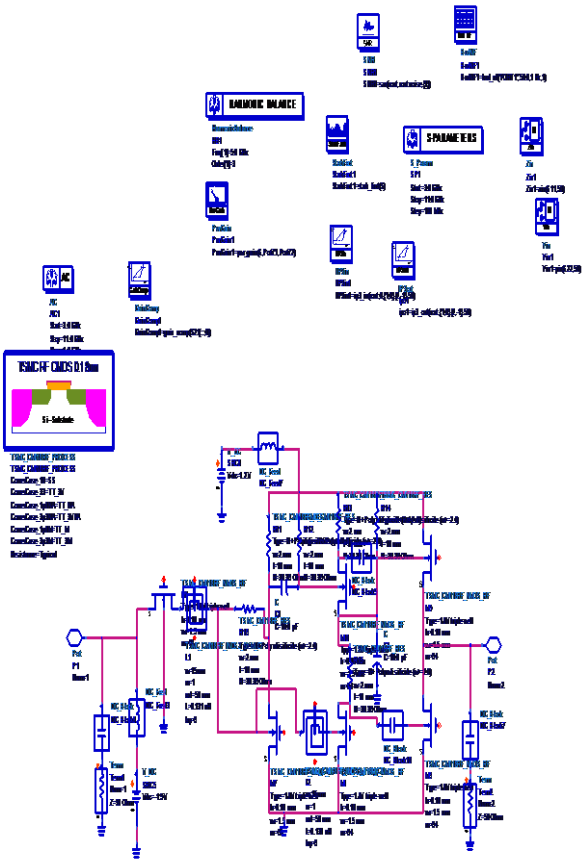


Fig. 2. Circuit Architecture Type Two

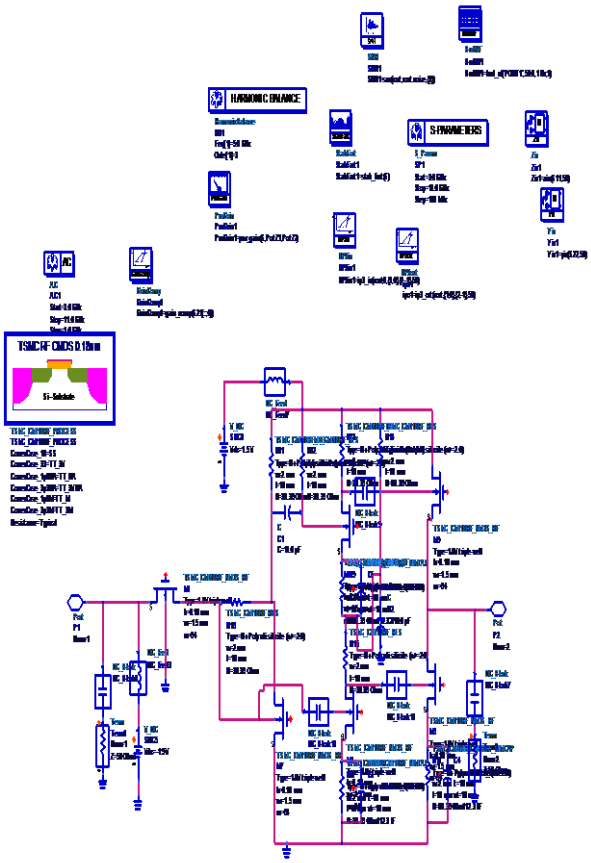


Fig. 3. Circuit Architecture Type Three

However, the on-chip inductor occupies a large silicon area. For applications where the area requirement is stringent, e.g., multiple-input multiple-output (MIMO) transceiver, the inductor- based design is not favorable, while the use of bond-wire inductance depends on the circuit configuration and is severely limited by the packaging and modeling technologies. Hence, in this paper, the capacitive peaking technique is employed for bandwidth extension, which has been successfully implemented in transimpedance amplifiers.

C. Circuit Architecture Type three

For the first order, provides an increasing regarding frequency. This effect can be understood conceptually from the resistive degeneration architecture. It is well known that a source-degenerative resistor degrades gain and improves linearity, while provides a signal path in parallel with to the ground. At high frequencies, the path through has a low impedance. Thus, the resistive degeneration effect is degraded by with the increase of frequency, resulting in an increasing gain characteristic. However, the gain cannot exceed the value of a common-source stage without source degeneration, which actually sets the upper bound of the gain of capacitive peaking stage. In other words, capacitive peaking is rather an approach to controlling the gain flatness at the cost of absolute gain value. Note that a negative impedance is created, therefore, the stability of the capacitive peaking LNA should be carefully examined.
Fig. 3 shows the final circuit of the proposed LNA.

IV. EXPERIMANTAL RESULTS

The simulation results are shown in Fig. 4-6.

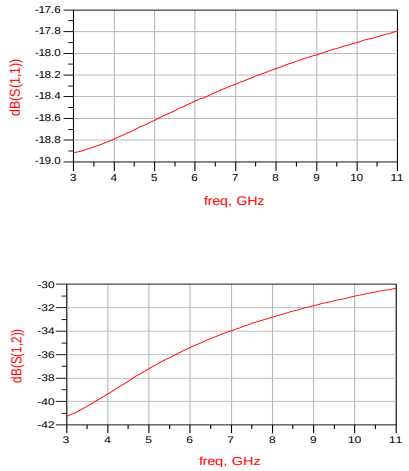
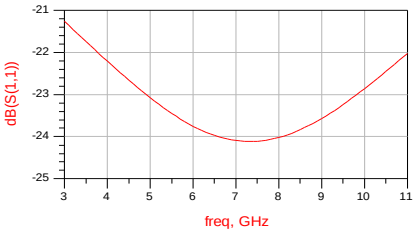


Fig. 4. Simulation of Circuit Type One



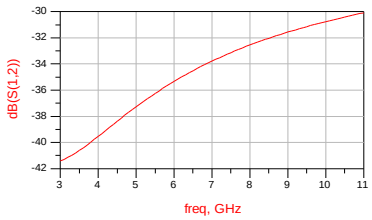


Fig. 5. Simulation of Circuit Type Two

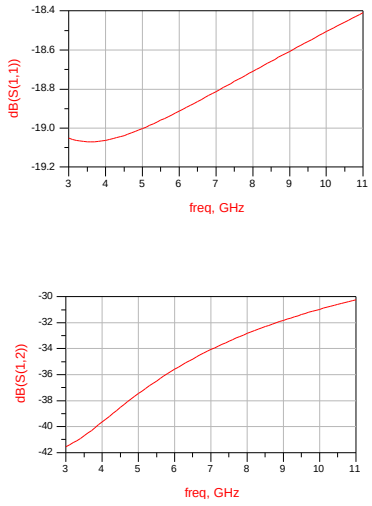


Fig. 6. Simulation of Circuit Type Three

With 1.5-V supply voltage, the circuit parameters are redesigned to preserve a similar condition. Results show that we have good matching in the implementations. capacitive peaking technique enhances gain flatness within 3 dB over 3–11 GHz. The stability is carefully verified, which shows the LNA is unconditionally stable.

V. Conclusion

This paper has demonstrated an inductorless LNA design capable of UWB applications. Without on-chip inductors, the ultra-wide 3-dB bandwidth was achieved by a syncretic adoption of thermal noise canceling, capacitor peaking, and current reuse. A gain-enhanced architecture based on the noise canceling principle was proposed and detailed analysis of this circuit was performed. Capacitive peaking is not able to enhance the absolute bandwidth; however, it is an effective way of controlling the gain flatness. Fabricated in a 0.18-µm triple-well CMOS process, the LNA achieves good matching in the implementations. Capacitive peaking technique enhances gain flatness within 3 dB over 3–11 GHz. The LNA consumes 19mW from a low supply voltage of 1.5 V. The performance is comparable and sometimes better than the reported inductor-based designs. Benefiting from its inductorless architecture, the LNA core occupies only a 0.05-mm2 die area, which is among the smallest UWB LNA reported in the literature.

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Maryam Vafadar was born in Iran in 1979. She received the B.S. degree in bioelectric engineering from Biomedical Engineering Faculty, Amirkabir University of Technology, Tehran, Iran, in 2002. In2008, she received M.S.degree in electronic from Electrical Engineering Faculty, Shahed University, Tehran, Iran. Currently, she is the teacher of Engineering Faculty, Islamshahr Azad University, Islamshahr, Iran.